Patent Claims

1. A field-effect transistor (222), having a doped channel region arranged along a depression (72), having a doped terminal region (16) near an opening of the depression (72), having a doped terminal region (18) remote from the opening, having a control region (172) arranged in the depression (72), and having an electrical insulating region (170) between the control region (172) and the channel region, the terminal region (18, 54) remote from the opening leading as far as a surface containing the opening or being electrically conductively connected to an electrically conductive connection leading to the surface.

2. The field-effect transistor (222) as claimed in claim 1, wherein the terminal regions (16, 18) contain the same dopant concentration and dopants of the same conduction type.

3. The field-effect transistor (222) as claimed in claim 1 or 2, wherein the channel region has a length (l) corresponding to at least two thirds of the depth of the depression (72).

4. The field-effect transistor (222) as claimed in one of the preceding claims, wherein the depression is a trench (72) or a hole.

5. The field-effect transistor (222) as claimed in one of the preceding claims, wherein the channel region lies on both sides of the trench (72) or along the entire periphery of the hole.

6. The field-effect transistor (222) as claimed in one of claims 1 to 4, wherein the channel region lies only on one side of the trench (72) or only along part of the periphery of the hole.

7. The field-effect transistor (222) as claimed in one of the preceding claims, wherein the terminal region (18) remote from the opening lies in the region of a plurality of depressions (75b, 352), preferably at least two or at least three depressions, in which control regions are arranged and at which channel regions and terminal regions (16c) near the openings are arranged,
and wherein the control regions and the terminal regions (16c) near the openings are in each case electrically connected in parallel (380).

8. The field-effect transistor (222) as claimed in one of the preceding claims, wherein the depression (72) for the control region and a depression (70, 76) filled with an electrical insulating material between the field-effect transistor (222) and an adjacent electrical component have the same depth.

9. The field-effect transistor (222) as claimed in one of claims 1 to 7, wherein the depression (72) for the control region has a smaller depth than a depression (70a, 76a) filled with an electrical insulating material between the field-effect transistor (222) and an adjacent electronic component.

10. The field-effect transistor (222) as claimed in one of the preceding claims, wherein the insulating region (170) has an insulating thickness of at least 15 nm, preferably 20 nm,
and/or wherein the distance (l) between the terminal regions (16, 18) along the depression (72) is at least 0.4 µm,

and/or wherein at least one terminal region (16, 18) has a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than 9 volts or greater than 15 volts, but preferably less than 30 volts.

11. The use of the field-effect transistor (222) as claimed in one of the preceding claims as driving transistor at a word line (272, 288) or a bit line (296) of a memory cell array (230), in particular of a flash memory of an EEPROM memory module.

12. The use of the field-effect transistor (222) as claimed in one of the preceding claims for switching a voltage having a magnitude of greater than 9 volts or greater than 15 volts, but preferably less than 30 volts.

13. A method for fabricating a field-effect transistor (222), in particular a field-effect transistor (222) as claimed in one of claims 1 to 12,
having the following steps to be performed without restriction by the order specified:
provision of a carrier material (10) having a surface to be processed,
formation of a terminal region (16) near the surface and a terminal region (18) remote from the surface,
formation of at least one depression (72), which leads from the terminal region (16) near the surface as far as the terminal region (18) remote from the surface or which leads from a region for the terminal region near the surface to a region for the terminal region remote from the surface,
production of an electrical insulating layer (170) in the depression (72),
introduction of an electrically conductive control region (172) into the depression (72).

14. The method as claimed in claim 13, wherein the formation of the terminal regions is performed before the formation of the depression and/or before the filling of the depression (72).

15. The method as claimed in claim 13 or 14, comprising the following step:
formation of a connecting region (54) from the terminal region (18) remote from the surface to the surface of the semiconductor layer (10).

16. The method as claimed in one of claims 13 to 15, wherein at least one insulating depression (70, 74, 76) is formed at the same time as the depression (72) for the control region.

17. The method as claimed in claim 16, wherein the insulating depression (70, 74, 76) is formed with the same depth as the depression (72) for the control region.

18. The method as claimed in claim 16, wherein the insulating depression (70a, 76a) is made deeper than the depression (72a) for the control region.

19. The method as claimed in claim 18, wherein the insulating depression is wider than the depression (72) for the control region at least in an upper section, and wherein the two depressions are formed in a common etching process in which wider depressions are etched considerably more deeply than narrower depressions.

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List of reference symbols

10, 10a	Silicon substrate
12, 12a	Oxide layer
14, 14a	Nitride layer
16, 16a, 16c	Drain region
18, 18a, 18c	Source region
20	Photoresist layer
22	Cutout
24	Arrow
50	Photoresist layer
52	Cutout
54, 54a, 54b	Connecting line
56	Arrow
60, 60a	Hard mask
62 to 68	Region
62a to 68b	Region
70 to 76	Trench
70a to 76a	Trench
70b to 76b	Trench
B1, B2	Width
100	Sacrificial oxide layer
102	Sacrificial nitride layer
120 to 126	Bottom oxide
130	Sacrificial polysilicon
140	Photoresist layer
142 to 146	Cutout
150	Insulating material
160	Photoresist layer
162	Cutout
170	Gate oxide
172	Amorphous silicon
180, 182	Channel region
200	Filling material
202, 204	Bottom
220 to 226	Vertical transistor
230	Memory cell array
232	Drive unit
234	Broken line

240 to 246	Terminal
250 to 256	Gate terminal
260	Memory cell
262	Arrow
264	Memory transistor
266	Drive transistor
268	Intermediate layer
270	Gate terminal
272	Word line
274, 276	Terminal
278	Terminal
280	Auxiliary line
282, 284	Terminal
286	Gate terminal
288	Word line
290, 292	Terminal
294	Terminal
296	Bit line
300	Rectangle
A1, A2	Insulating width
L1	Trench length
310 to 314	Source contact
320 to 326	Drain contact
340, 342	Substrate contact
350	Vertical field-effect transistor
352	Trench
360 to 366	Sidewall
370 to 376	Arrow
380, 382	Connection
1	Channel length
400 to 404	Vertical transistor